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| 09/594,205 | 06/14/2000 | Jonathan Huie | SIA-P008 | 8285 |

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Michael L Gencarella Esq
Martine & Penilla LLP
710 Lakeway Drive #170
Sunnyvale, CA 94085

| EXAMINER |
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DELGADO, MICHAEL A

| ART UNIT | PAPER NUMBER |
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2144

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/594,205

Applicant(s)

HUIE ET AL.

Examiner

Michael S. A. Delgado

Art Unit

2144

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 April 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No.

6,460,120 by Bass et al and US Patent No. 5,666,494 by Mote Jr. in view of IEEE public

""Routing Lookups in Hardware at Memory Access Speeds", IEEE Infocom, April 1998 by

Gupta et al.

In claim 1, Bass teaches about a high performance network address processor comprising (Fig 1):

a longest prefix match lookup engine for receiving a network address request having a designated network destination address (Col 7, line 60-Col 8, line 15), and

an associated data engine "Data Store Coprocessor" coupled to the longest prefix match lookup engine "Tree Search Engine Coprocessor" that is capable of receiving a key and an output address pointer "forwarding information" from the longest prefix match lookup engine

Art Unit: 2144

and that is capable of providing a network address processor “protocol processor” data output corresponding to the designated network address pointer (The leaf contains destination address) (Col 7, line 60-Col 8, line 15), (Col 8, line 65-Col 9, line 10) (Col 25, lines 35-50) (Col 27, lines 1-10).

But does not explicitly teach about the longest prefix match lookup table having multiple pipelined lookup tables, a first pipelined lookup table having a single row of a first set of data pairs, a second pipelined lookup table having a plurality of rows of a second set of data pairs.

Gupta disclosed a pipeline operation used in a network router application in which multiple lookup tables were used to increase the throughput (Fig 4) (Section 3, lines 1-16).

Mote taught about the advantage of having a large number of columns in a single row to increase memory access speed (Col 1, lines 25-40).

Bass disclosure taught about the importance of efficient search in locating forwarding addresses in order to reducing the bottlenecks in network routing (Col 2, lines 25-40) (Col 3, lines 1-5). To solve the bottleneck problem, a pipeline approach was disclosed (Col 3, lines 1-5). By using the pipeline approach of Gupta with the first lookup table being a single row as in the case of Mote invention, the time taken when accessing a router-mapping table will be reduced.

It would have been obvious for some one of ordinary skill at the time of the invention to use the combine approach of Gupta and Mote in order to reduce the access time when searching for a network forwarding address.

In claim 2, Bass combined with Gupta and Mote, teaches about a high performance network address processor of claim 1 wherein the longest prefix match lookup engine a third

Art Unit: 2144

pipelined lookup table having a plurality of rows of a third set of data pairs (Bass Col 20, line 65-Col 21, line 5) (Gupta section 4, lines 1-20).

In claim 3, Bass combined with Gupta and Mote, teaches about a high performance network address processor of claim 1 wherein a value representing a position of a selected element in the single row of a first set of data pairs is an input to the second pipelined lookup table the input used to select one of the plurality of rows of the second set of data pairs (Gupta Fig 6) (Covered in claim1).

In claim 4, Bass combined with Gupta and Mote, teaches about a high performance network address processor of claim 2 wherein a value representing a position of a selected element in the single row of a first set of data pairs is a first input to the second pipelined lookup table the input used to select one of the plurality of rows of the second set of data pairs, a second input into the second pipelined lookup table is used to locate one of the data pairs of the one of the plurality of rows (Gupta Fig 2) (Gupta section 3, lines 1-16).

In claim 5, Bass combined with Gupta and Mote, teaches about a high performance network address processor integrated circuit, wherein the network address processor integrated circuit comprises (Fig 1):

a longest prefix match lookup engine "Tree Search Engine Coprocessor" for receiving a network address request having a designated network destination address, the longest prefix match lookup table engine having a plurality of pipelined lookup tables (Col 7, line 60-Col 8, line 15) (Gupta section 3, lines 1-16); and

an associated data engine "Data Store Coprocessor" coupled to the longest prefix match lookup engine "Tree Search Engine Coprocessor" that is capable of receiving a key value and

Art Unit: 2144

an output address pointer “forwarding information” from longest prefix match lookup engine and that is capable of providing a network address processor “protocol processor” data output corresponding to the designated network address pointer, the associated data engine having a first lookup table having a plurality of rows wherein a portion of bits of the key value is used to select one of the plurality of rows as an output, a remaining portion of the bits of the key value identifying a row in a second lookup table having a plurality of rows (Bass Col 7, line 60-Col 8, line 15), (Bass Col 8, line 65-Col 9, line 10) (Bass Col 25, lines 35-50) (Bass Col 27, lines 1-10) (Gupta section 3, lines 1-16) (covered in claim 1).

In claim 6, Bass combined with Gupta and Mote, teaches about a high performance network address processor of claim 5 wherein the longest prefix match lookup engine comprises a third pipelined lookup table having a plurality of rows of a third set of data pairs (Bass Col 20, line 65-Col 21, line 5) (Gupta section 4, lines 1-20).

In claim 7, Bass combined with Gupta and Mote, teaches about a high performance network address processor of claim 5 wherein a value representing position of a selected element in the single row of a first set of data pairs is an input to the second pipelined lookup table, the input used to select one of the plurality of rows of the second set of data pairs (Gupta section 3, lines 1-16).

In claim 8, Bass combined with Gupta and Mote, teaches about a high performance network addressing method comprising the steps of (Fig 1):

Art Unit: 2144

providing a longest prefix match lookup engine “Tree Search Engine Coprocessor” with a network address data request and a destination network address, wherein the longest prefix match lookup engine comprises a set of lookup tables (Bass Col 7, line 60-Col 8, line 15), (Bass Col 20, line 65-Col 21, line 5);

successively searching the set of lookup tables to select a look up engine address output from the set of lookup tables (Bass Col 7, line 60-Col 8, line 15);

selecting a position within a row of a first lookup table(Gupta Fig 6) (Gupta section 4, lines 1-20);

identifying a value associated with the position(Gupta Fig 6) (Gupta section 4, lines 1-20);

utilizing, the value as a first input to a second lookup table(Gupta Fig 6) (Gupta section 4, lines 1-20);

selecting a row of the second lookup table according to the first input(Gupta Fig 6) (Gupta section 4, lines 1-20);

selecting a position within the row of the second lookup table according to a second input(Gupta Fig 6) (Gupta section 4, lines 1-20); and

accessing a value stored in the position within the row of the second lookup table; (Gupta Fig 6) (Gupta section 4, lines 1-20);

defining a pointer to provide as input to an associated data engine(Gupta Fig 6) (Gupta section 4, lines 1-20); and

searching the associated data engine “Data Store Coprocessor” to provide an associated destination address data output (Bass Col 7, line 60-Col 8, line 25).

Art Unit: 2144

In claim 9, Bass combined with Gupta and Mote, teaches about a high performance network addressing method of claim 8 wherein successively of searching the set of lookup tables comprises searching for an entry of the set of lookup tables that comprises the smallest entry that is greater than or equal to an input search key (Bass Col 7, line 60-Col 8, line 15):

selecting the smallest entry that equals the input search key with a corresponding number of mask bits, wherein if one or more entries comprise the same key, the key having the smallest mask is selected (Bass Col 25, line 45-Col 26, line 5); and

wherein if no key matches, the maximum key in a row is compared with the input search key using each of a set of respective mask pointer pairs, of the pointer is selected to correspond to the smallest mask for which the input search key equals the maximum key in a row of a corresponding lookup table with the corresponding number of mask bits ignored (Bass Col 25, line 45-Col 26, line 5).

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

Art Unit: 2144

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US patent No. 6,539,369 by Brown, teaches about a method and apparatus for storing sparse and dense subtrees in a longest prefix match lookup table.

US patent No. 6,460,112 by Srinivasan et al, teaches about a method and apparatus for determining a longest prefix match in a content addressable memory device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael S. A. Delgado whose telephone number is (571) 272-3926. The examiner can normally be reached on 7.30 AM - 5.30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A. Wiley can be reached on (571) 272-3923

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.


Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 09/594,205
Art Unit: 2144

Page 9

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MD

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DAVID WILEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100